ABSTRACT OF THE INVENTION

According to one aspect of the invention, a method is provided in which a write strobe signal is generated to latch output data into a memory unit that comprises one or more dual data rate synchronous dynamic random access memory (DDR-SDRAM) devices. The write strobe signal has an edge transition at approximately the center of a data window corresponding to the output data. A first receive clock signal is delayed by a first delay period using a delay locked loop (DLL) circuit to generate a first delayed receive clock signal. The first delayed receive clock signal is used to latch incoming data from the memory unit.